**STRS Application Repository Submittal Checklist for \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

| **Item** | **STRS Requirement ID** | **STRS Application Repository Submission** | **Filenames** | **Additional Information** | **Submitted?** |
| --- | --- | --- | --- | --- | --- |
| 1 |  | NASA only: Submit Disclosure of Invention and New Technology (Including Software) form, using the new technologies reporting website at <https://invention.nasa.gov/> . |  |  |  |
| 2 |  | SBIR/STTR Contractors: Submit Disclosure of Invention and New Technology (including Software) form using the [Electronic Handbook (EHB).](https://ehb8.gsfc.nasa.gov/sbir) |  |  |  |
| 3 |  | NASA only: Submit NASA Software Release Request Authorization (SRRA); see Software Release System at <https://softwarerelease.ndc.nasa.gov/>. |  |  |  |
| 4 |  | Submit any available checklist showing that your internal procedures were followed. NASA only: Fill in NPR 7150.2 Requirements Compliance Matrix; see NASA Software Release System at <https://softwarerelease.ndc.nasa.gov/>. |  |  |  |
| 5 |  | Submit Public Metadata from web form at https://strs.grc.nasa.gov/repository/forms/public-metadata/. The Public Metadata submitted will describe the application, which will be available for retrieval on the STRS website. |  |  |  |
| 6 |  | Submit Restricted Metadata from web form at <https://strs.grc.nasa.gov/repository/forms/restricted-metadata/>. The Restricted Metadata submitted will describe the contact information of the people involved in the creation of the application, this information will not be available for retrieval. |  |  |  |
| 7 | STRS-12(1) | Submit application or OE or system component software and configurable hardware design simulation model(s) and/or documentation. (Usually in Design Description Document but may be machine readable.) |  |  |  |
| 8 | STRS-12(2) | Submit documentation of external interfaces for STRS application, devices, or configurable hardware design (e.g., signal names, descriptions, polarity, format, data type, and timing constraints). (Usually in HID) |  |  |  |
| 9 | STRS-12(3) | Submit documentation of STRS application or OE behavior and adaptability (e.g., configurable and queryable data items). (Usually in Design Description Document, User’s Guide) |  |  |  |
| 10 | STRS-12(4) | Submit application or OE function sources (e.g., C, C++, header files, very-high-speed integrated circuit HDL (VHDL), and Verilog). (Usually in Artifacts) |  |  |  |
| 11 | STRS-12(5) | Submit application or OE libraries, if applicable (e.g., electronic design interchange format (EDIF), dynamic link library (DLL)). (Usually in Artifacts) |  |  |  |
| 12 | STRS-12(6) | Submit documentation of application or OE development environment and/or tool suite as follows: (Usually in Design Description Document) |  |  |  |
| 13 | STRS-12(6A) | A.    Include the development environment and/or tool suite name, purpose, developer, version, and configuration specifics (e.g., ISE Design Suite System, Xilinx, 14.4, EDK and SDK; MATLAB®, Model base design support automatic code generation, MathWorks, R2016a). |  |  |  |
| 14 | STRS-12(6B) | B.    Include a description of the hardware on which the development environment and/or tool suite is executed, its OS, OS developer, OS version, and OS configuration specifics (e.g., Microsoft® Windows 7, Service pack 2; Linux® Ubuntu, (Xenial Xerus) 16.04). |  |  |  |
| 15 | STRS-12(6C) | C.    Include a description of the output of the development environment and/or tool suite, its STRS infrastructure/OE description, developer, version, and unique implementation items (e.g., Type of file, .mdl, .slx; GRC's STRS Reference Implementation; IP generated from Xilinx). |  |  |  |
| 16 | STRS-12(6D) | D.    Include a description of licensing agreements for development environment and/or tool suite. |  |  |  |
| 17 | STRS-12(7) | Submit test plans, procedures, and results documentation. (Usually in V&V Plan, V&V Procedure, and V&V Results) |  |  |  |
| 18 | STRS-12(8) | Submit identification of software development standards used, for example, NPR 7150.2A. (Usually in Version Description Document (VDD)/Metadata) |  |  |  |
| 19 | STRS-12(8) | Submit identification of software development standards used, for example, CMMI 1.3 Level 2. |  |  |  |
| 20 | STRS-12(9) | Submit version of STRS Standard used. (e.g.: v1.02.1, NASA-STD-4009) (Usually in VDD/Metadata) |  |  |  |
| 21 | STRS-12(10) | Submit information, along with supporting documentation, required to make the appropriate decisions regarding ownership, distribution rights, and release (technology transfer) of the application or OE and associated artifacts. (Transfer Rights/Agreements) |  |  |  |
| 22 | STRS-12(11) | Submit version description document if available, or other document containing the version number of each separable artifact in the release, defined down to the lowest level components. (Usually in VDD) |  |  |  |
| 23 | STRS-12(12) | Submit documentation of the platform component hardware used by the application or OE, its function and the interconnections. If the component executes an operating system, document the OS, OS developer, OS version, and OS configuration. (Usually in HID) |  |  |  |
| 24 | STRS-12(13) | Submit documentation when an OE is submitted to the STRS Application Repository, providing guidelines to aid a waveform/application developer and integrator in the task of developing an STRS compliant waveform/application. (Usually in OE-Specific Developer’s Guide) |  |  |  |
| 25 | STRS-14 | Submit platform-specific wrapper for each user-programmable FPGA. (STRS-14) The STRS SPM developer shall provide a platform-specific wrapper for each user-programmable FPGA, which performs the following functions: (1) Provides an interface for command and data from the GPM to the waveform application. (2) Provides the platform-specific pinout for the STRS application developer. This may be a complete abstraction of the actual FPGA pinouts with only waveform application signal. |  |  |  |
| 26 | STRS-15 | Submit platform-specific wrapper documentation. (STRS-15) The STRS SPM developer shall provide documentation on the configurable hardware design interfaces of the platform-specific wrapper for each user-programmable FPGA, which describes the following: (1) Signal names and descriptions. (2) Signal polarity, format, and data type. (3) Signal direction. (4) Signal-timing constraints. (5) Clock generation and synchronization methods. (6) Signal-registering methods. (7) Identification of development tool set used. (8) Any included noninterface functionality. |  |  |  |
| 27 |  | Submit agreements, contracts, and copyrights, for proprietary, usage, ownership, warranty, licensing, and transfer rights, which support or restrict reuse. |  |  |  |
| 28 |  | Optional - Submit any Lessons Learned, from web form at <https://strs.grc.nasa.gov/repository/forms/lessons-learned/>. |  |  |  |
| 29 |  | STRS Repository Manager creates detailed application artifact metadata using the Python script at <https://strs.grc.nasa.gov/repository/script-library/getartifactmetadata/>; forward CSV file to submitter to edit; save edited response. |  |  |  |
| 29 |  | Submitter edits application artifact metadata created by the STRS Repository Manager, named Artifact.yyyymmddhhmmss.csv to remove the TBDs. Usually edit with Excel. Send back to STRS repository manager (<mailto:strs-repository-manager@lists.nasa.gov?subject=Artifact%20Metadata>). |  |  |  |
| 30 |  | If known: Submit any available STRS compliance testing results, in consultation with the STRS compliance certification team ([mailto:strs@lists.nasa.gov](mailto:strs@lists.nasa.gov?STRS%20Compliance)). |  |  |  |

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